Abstract of the Disclosure

A nonvolatile semiconductor memory device has a memory cell array having a memory cell and arranged in an array shape by connecting this memory cell to a bit line and a word line, an address input terminal inputting an address thereto, and a test mode circuit for outputting a test mode signal when a signal is inputted to a predetermined terminal among this address input terminal. The nonvolatile semiconductor memory device further has a row decoder connected to the test mode circuit and applying a voltage for a test to all the word lines in response to the test mode signal, a column decoder connected to the test mode circuit and setting all the bit lines to a non-selecting state in response to the test mode signal, and a monitor terminal connected to the test mode circuit and outputting the test mode signal.